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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,047	03/18/2004	Der-Zheng Liu	BHT-3111-441	4615

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EXAMINER
PERILLA, JASON M

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
08/22/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
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Office Action Summary	Application No.	Applicant(s)	
	10/803,047	LIU ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2611	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *5,15,21 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-14,16-20 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are pending in the instant application.

Election/Restrictions

2. This application contains claims directed to the following patentably distinct species:

I. Claims 1-5, 10-15, 18, 21, and 22 the embodiment of figures 4 and 5, drawn to sampling timing compensation accomplished via control of a cyclic prefix remover, classified in class 375, subclass 362.

II. Claims 1-4, 6-14, 16-20, and 23, the embodiment of figures 6 and 7, drawn to sampling timing compensation accomplished via control of a ADC sampling device, classified in class 375, subclass 355.

Applicant is required under 35 U.S.C. § 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, claims 1-4, 10-14, and 18 are generic.

3. Applicant's election without traverse of claims 1-4, 6-14, 16-20, and 23 in the reply filed on August 10, 2007 is acknowledged.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. § 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

5. Claims 3, 4, and 7 are objected to because of the following informalities:

Regarding claim 3, in line 4, "calculating a timing offset" should be replaced by –calculating the timing offset--, and, in line 5, "a difference of the first" should be replaced by –a difference between the first--.

Regarding claim 4, in line 1, "the symbol" is lacking antecedent basis.

Regarding claim 7, in line 1, "wherein period" should be replaced by –wherein a period--, and, in line 2, "than the sampling" should be replaced by –than a sampling--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 1-4, 6, 10-14, 16, 18-20, and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Gilbert et al (U.S. Pat. No. 7123670; hereafter "Gilbert") in view of Singh et al (U.S. Pat. No. 7139320; hereafter "Singh").

Regarding claim 1, Gilbert discloses an apparatus for timing compensation (abstract) at a receiver (fig. 7) of a communication system, wherein each of a first symbol and a second symbol comprising at least two pilot signals transmitted via a first and a second pilot subchannels respectively, and the first and the second pilot subchannels comprise a first and a second pilot indexes respectively (col. 12, lines 20-30), the apparatus comprising: a pilot subchannel estimator for generating a frequency response of the first and the second symbols according to the pilot signals of the first

and the second symbols respectively (fig. 7, refs. 705, 710, and 712; col. 12, lines 40-53); a timing offset estimator (fig. 7, ref. 720), coupled to the pilot subchannel estimator, for calculating a timing offset (col. 13, lines 3-28), wherein the offset is generated according to the frequency responses of the first and the second symbols; and a phase rotator (fig. 7, refs. 422 and 420), coupled to the timing offset estimator, for performing timing compensation according to a phase rotation corresponding to the timing offset (col. 13, lines 33-37). Gilbert discloses, in a multicarrier OFDM receiver (col. 1, lines 55-65), correcting for an error caused by an offset in frequency between the transmitter and receiver (col. 2, lines 35-40). The pilot subchannel estimator determines a frequency response (via FFT block; fig. 7, ref. 705) of a first pilot index of a first subchannel and stores it in memory (fig. 7, ref. 712) for division (fig. 7, ref. 710) with a determined frequency response of a second pilot index of a second subchannel. Thereafter, the timing offset estimator determines a "phase difference between the phase in a pilot carrier of the first data symbol and the phase in the corresponding pilot carrier of the second data symbol" (col. 13, lines 7-9). Finally, Gilbert discloses the phase rotator for correcting the offset.

Gilbert discloses determining a phase difference between the pilot symbols of two subcarriers of a multicarrier system. Such difference is indicative of a frequency offset between the transmitter and the receiver. However, although one skilled in the art is aware that such offset is manifested in the receiver due to poor synchronization of the receiver's local oscillation frequency (i.e. fig. 7, ref. 416) and sampling frequency (fig. 7, ref. 418) with respect to the operating frequency of the transmitter, Gilbert does not

explicitly disclose the correction of a sampling frequency offset. However, Singh discloses, in a strictly analogous sampling timing compensation apparatus (fig. 4), compensating both the downconverter frequency (fig. 4, ref. 32) and sampling timing frequency (fig. 4, ref. 34; col. 8, lines 45-55) according to the determined pilot offset (col. 8, lines 15-35). Singh's compensation is performed for frequency synchronization between the OFDM transmitter and receiver (col. 8, lines 52-55). Therefore, it would have been obvious at the time the invention was made that Gilbert's determination of phase offset could be advantageously utilized to update the downconverter frequency (Gilbert; fig. 7, ref. 416) and sampling frequency (Gilbert; fig. 7, ref. 418) as taught by Singh because it would achieve frequency synchronization between the OFDM transmitter and receiver.

Regarding claim 2, Gilbert in view of Singh disclose the limitations of claim 1 as applied above. Further, Gilbert discloses a multi-carrier system as applied above.

Regarding claim 3, Gilbert in view of Singh disclose the limitations of claim 1 as applied above. Further, Gilbert discloses that the timing offset estimator further comprises a phase difference calculating device for calculating a phase difference between the frequency responses of both the first and the second symbols, and a divider for calculating the timing offset through dividing the phase difference by a difference between the first and the second pilot indexes (col. 12, lines 25-30). The pilot indexes are determined according to their position in time. Hence, "the time elapsed between the two data symbols" is associated with the pilot indexes.

Regarding claim 4, Gilbert in view of Singh disclose the limitations of claim 4 as applied above. Further, Gilbert discloses the use of more than two subchannels (col. 1, lines 55-65), the timing offset estimator further comprises a phase difference calculating device (col. 12, lines 25-30) for calculating at least two phase differences between the frequency responses of at least two pairs of the symbols respectively; a divider (col. 12, lines 25-30) for dividing each of the phase differences by a difference of the pilot indexes of the subchannels transmitting the corresponding symbols (also as applied to claim 3 above); and an timing offset calculating device for calculating the timing offset through averaging the dividing results (col. 13, lines 10-15).

Regarding claim 6, Gilbert in view of Singh discloses the limitations of claim 1 as applied above. Further, Singh discloses a timing controller (fig. 4, output of 80) for generating a control signal ("FREQUENCY SYNCH ADJUSTMENT") according to the timing offset, wherein the phase of the sampling clock (fig. 4, ref. 82) is adjusted according to the control signal; and an analog-to-digital converter (ADC) (fig. 4, ref. 34) for converting the symbol according to the sampling clock.

Regarding claim 10, Gilbert in view of Singh disclose the limitations of the claim as applied to claim 1 above.

Regarding claim 11, Gilbert in view of Singh disclose the limitations of claim 10 as applied above. Further Gilbert in view of Singh disclose the remaining limitations of the claim as applied to claim 3 above.

Regarding claim 12, Gilbert in view of Singh disclose the limitations of claim 11 as applied above. Further Gilbert in view of Singh disclose the remaining limitations of the claim as applied to claim 3 above.

Regarding claim 13, Gilbert in view of Singh disclose the limitations of claim 10 as applied above. Further Gilbert in view of Singh disclose the remaining limitations of the claim as applied to claim 4 above.

Regarding claim 14, Gilbert in view of Singh disclose the limitations of claim 13 as applied above. Further Gilbert in view of Singh disclose the remaining limitations of the claim as applied to claim 4 above.

Regarding claim 16, Gilbert in view of Singh disclose the limitations of claim 10 as applied above. Further Gilbert in view of Singh disclose the remaining limitations of the claim as applied to claim 6 above.

Regarding claim 18, Gilbert in view of Singh disclose the limitations of the claim as applied to claim 1 above. Further Gilbert in view of Singh disclose a pre-FFT processing device for processing in the time domain (Singh; fig. 4, refs. 32, 34), a FFT for transforming the symbols to the frequency domain (Gilbert; fig. 7, ref. 424), and a, adjusting device for adjusting the operation of the pre-FFT processing device (Singh; fig. 4, ref. 82).

Regarding claim 19, Gilbert in view of Singh disclose the limitations of claim 18 as applied above. Further, Singh discloses that the pre-FFT processing device includes an ADC as applied in claim 18 above.

Regarding claim 20, Gilbert in view of Singh disclose the limitations of claim 19 as applied above. Further, Singh discloses that the pre-FFT processing device further includes a timing controller (fig. 4, output of 80) for generating a control signal ("FREQUENCY SYNCH ADJUSTMENT") according to the timing offset and a clock generator (fig. 4, ref. 82) for controlling the operation of the ADC (fig. 4, ref. 34).

Regarding claim 23, Gilbert in view of Singh disclose the limitations of the claim as applied to claim 1 above.

8. Claims 7, 8, and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Gilbert in view of Singh, and in further view of National ("Application of the ADC1210 CMOS A/D Converter"; National Semiconductor Application Note 245, April 1986).

Regarding claim 7, Gilbert in view of Singh disclose the limitations of claim 6 as applied above. Gilbert in view of Singh do not explicitly disclose that the period of the sampling clock (Tf) is shorter than a sampling interval (Ts) of the ADC. However, it is notoriously known in the art that many modern ADC converters require multiple clock periods to convert an analog signal into a high resolution binary number. Such ADC converters operate in a type of serial fashion to save cost. Specifically, National discloses, on the second column of page 5, that a 500kHz clock could be utilized by the disclosed ADC to create a 12 bit digital representation of an analog signal in 26us. That is, the period of the sampling clock (a 500kHz clock has a 2us period) is more frequent (shorter) than the sampling output interval (every 26us). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made

to utilize a serial fashion output ADC converter as disclosed by National having a longer sampling interval than sampling clock interval in the apparatus of Gilbert in view of Singh because it would save cost.

Regarding claim 8, Gilbert in view of Singh, and in further view of National disclose the limitations of claim 7 as applied above. Further, Gilbert in view of Singh, and in further view of National disclose the remaining limitations of the claim as applied in claim 7 above.

Regarding claim 17, Gilbert in view of Singh disclose the limitations of claim 13 as applied above. Further Gilbert in view of Singh, and in further view of National disclose the remaining limitations of the claim as applied to claim 7 above.

9. Claim 9 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Gilbert in view of Singh, and in further view of Matheus et al (U.S. Pat. No. 7009932; hereafter "Matheus").

Regarding claim 9, Gilbert in view of Singh disclose the limitations of claim 6 as applied above. Gilbert in view of Singh do not disclose, however, that the clock generator (Singh; fig. 4, ref. 82) comprises a PLL. Rather, Singh illustrates and discloses a Numerically Controlled Oscillator (NCO). However, the use of phase locked loop circuits as oscillators is notoriously known in the art as taught and disclosed by Matheus (fig. 5, ref. "CORR1"; col. 15, lines 10-12). Therefore, it would have been obvious to one having ordinary skill in the art at the time that the invention was made to utilize a PLL in place of Singh's NCO to generate a clock signal because the use of a PLL is well known and accepted in the art.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art not relied upon above is cited to further show the state of the art with respect to

U.S. Pat. No. 7058002 to Kumagai et al.

U.S. Pat. No. 6928120 to Zhang

U.S. Pub. No. 2003/0108127 to Eilts et al.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jason M. Perilla
August 14, 2007

jmp

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER